Total No. of Questions : 08]

SEAT No. :

P2005

[Total No. of Pages : 2

[5059] - 601
B.E. (Electronics) (End-Semester)
VLSI DESIGN
(2012 Pattern)

Time : $2\frac{1}{2}$ *Hours]* *[Max. Marks : 70*

Instructions to the candidates:

1) ***Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of Calculator is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Explain different architectural modeling types in VHDL give examples of each. **[8]**

b) Compare CPLD with FPGA. **[6]**

c) Draw FSM diagram and write VHDL code for 1100 Moore sequence. **[6]**

OR

Q2) a) Write a VHDL code for 4 bit Up down counter. Also write test bench for it. **[8]**

b) Draw block diagram and explain architecture of CPLD. **[6]**

c) Draw CMOS inverter and explain voltage transfer curve in detail. **[6]**

Q3) a) Explain read write operation of 6T SRAM cells with help of timing diagram. **[8]**

b) Give Classification of memories with application of each **[8]**

OR

Q4) a) Draw and explain DRAM in detail (any two schematics). **[8]**

b) Explain refresher circuit and sense amplifier. **[8]**

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Q5) a) Explain global and switch box routing. **[8]**

b) Explain off chip connections and I/O pad architecture **[8]**

OR

Q6) a) Explain power and ground distribution in detail. **[8]**

b) Explain floor planning. Purpose and rules? **[8]**

Q7) a) With reference to BIST explain BILBO, LFSR, CUT, scan chain for flipflops. **[10]**

b) What are the different faults in chip design? What are the techniques to minimize them. **[8]**

OR

Q8) a) Explain TAP controller with its state diagram. **[10]**

b) What is need of boundary scan? Explain Boundary scan technique in detail. **[8]**

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